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EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,011	SEDLAK ET AL.	
	Examiner	Art Unit	
	Kevin P Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/10/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3 and 4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3 and 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 3-4 have been examined.

2. Acknowledgement of the following papers filed: Amendment as received on 2/10/06. The papers filed have been placed on record.

Withdrawn Claim Rejections

3. All rejections and/or objections regarding claims 1-2, 5-7 have been withdrawn in response to the amendment canceling said claims.

Apparatus with Functional Language

4. Applicant's attention is directed towards MPEP 2114 [R-1] "Apparatus and Article Claims — Functional Language", which is copied below for Applicant's convenience. The independent claims are directed towards an apparatus (microprocessor) and multiple instances of functional language are found in the claims. For instance, "a memory *for storing an instruction length*". There does not appear to be any structural difference between an ordinary memory and the claimed "memory *for storing an instruction length.*" Furthermore, "a multiplexer having a first input, a second input *for receiving a 0 value...*" There does not appear to be any structural difference between an ordinary multiplexer input and a multiplexer input *for receiving a zero.* Limitations in an apparatus claim must structurally distinguish the claimed invention from the prior art.

MPEP 2114 [R-1] Apparatus and Article Claims — Functional Language

APPARATUS CLAIMS MUST BE STRUCTUR-ALLY DISTINGUISHABLE FROM THE PRIOR ART

>While features of an apparatus may be recited either structurally or functionally, claims< directed to >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429,1431-32 (Fed. Cir. 1997) (The absence of a disclosure in a prior art reference relating to function did not defeat the Board's finding of anticipation of claimed apparatus because the limitations at issue were found to be inherent in the prior art reference); see also In re Swinehart, 439 F.2d 210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971);< In re Danly, 263 F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). "[A]pparatus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original).

MANNER OF OPERATING THE DEVICE DOES NOT DIFFERENTIATE APPARATUS CLAIM FROM THE PRIOR ART

A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987) (The preamble of claim 1 recited that the apparatus was "for mixing flowing developer material" and the body of the claim recited "means for mixing..., said mixing means being stationary and completely submerged in the developer material". The claim was rejected over a reference which taught all the structural limitations of the claim for the intended use of mixing flowing developer. However, the mixer was only partially submerged in the developer material. The Board held that the amount of submersion is immaterial to the structure of the mixer and thus the claim was properly rejected.)

New Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 3 and 4 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. "A computation unit for computing relative addresses" has not been described sufficiently to enable one skilled in the art to make and/or use the invention. The claimed invention calls for, "a

multiplexer...***a computation unit***...[and] an ***adding unit connected between*** said program counter ***and said computation unit***, said ***adding unit*** having...***an output connected to said computation unit***." (Emphasis added by Examiner)

However, Applicant has argued:

> "Contrary to Applicants' claimed invention, a **complicated cascade of adding units** is necessary in Yoshida, **in order to compute the correct value for determining the relative address on the basis of the program code**. Thus, Yoshida, like Goetz fails to teach or suggest, among other limitations of Applicants' claims, the controlled supplying of instruction word lengths or the value 'o', to a multiplexer, in dependence upon which assembler code is selected. "

Thus is appears Applicant regards the claimed "computation unit" as something less complicated than the adding unit, as that is the difference between the "cascade of adding units" and the "adding unit...connected to said computation unit". It is unclear to the Examiner how the claimed invention's arrangement of adding unit and computation unit differs from Yoshida's disclosed "complicated cascade of adding units". However, Applicant has argued the claimed invention and the "complicated cascade of adding units" of Yoshida are different from each other yet the specification does not provide details to enable one of ordinary skill in the art to make/use a "computation unit for computing relative addresses" without using an adder as disclosed in Yoshida and as is well known in the art.

Maintained Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been

obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goetz, U.S. Patent 5,854,913 in view of Yoshida, U.S. Patent 4,926,323, Logic and Computer Design Fundamentals by Mano and Kime, The PowerPC Architecture, 1994 and K. Short, Embedded Microprocessor Systems Design, 1998.

9. As per claim 3, Goetz discloses:

- A microprocessor for processing various assembler codes: (Abstract, line 1)

- Depending on how the parameter is set, a different relative addressing takes place: (Relative addressing is defined as, "An addressing mode in which the effective address is formed by adding an offset to the program counter (or a portion thereof) during execution." (The Authoritative Dictionary of IEEE Standards Terms) Therefore, incrementing a program counter is relative addressing, because the program counter has a current value, and a new value is reached by adding an instruction length to the current PC address. Since the Q-bit indicates different instruction lengths to be added to the current PC address, different relative addressing takes place dependent on the Q-bit (Figure 9, Column 16, lines 47-64). Column

- A program counter (NIFA Compute 807, figure 9 and column 16, lines 47-64)

- A computation unit for computing relative addresses: (NIFA Compute 807, figure 9 and column16, lines 47-64)

10. While Goetz teaches multiple instruction sets being implemented and indicated by a parameter, Goetz is silent on how the different offsets for branch instructions are handled. It is well known in the art that PowerPC branch instructions add an offset to the address of the branch instruction (Page 36, numeral 1, The PowerPC Architecture), while x86 branch instructions add an offset to the address of the instruction following the branch instruction (Short, Embedded Microprocessor Systems Design, page 190, 2nd paragraph). However, since Goetz is silent on how the above issue is resolved, Goetz fails to teach:

- A multiplexer having a first input a second input for receiving a zero value, a third input receiving a parameter designating a respective assembler code, a memory for storing an instruction length having an output connected to said first input of said multiplexer
- An addition unit connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a second input for an instruction length, and an output connected to said computation unit:

11. Yoshida teaches hardware to implement an x86-like branch instruction, which adds an offset to the address of the instruction following the branch instruction:

- A program counter (register 13, figure 2; Column 4, lines 8-20)

- A computation unit for computing relative addresses: (2nd Adder 17, figure 2 and column 4, lines 1-20)

- An addition unit connected between said program counter and said computation unit: (1st Adder 15)

-Said adding unit having a first input connected to said program counter, a second input for an instruction length, and an output connected to said computation unit: (Figure 2, the 1st adder 15 has the program counter (register 13) as an input, has an input for an instruction length ("Word Length"), and has an output connected to said computation unit (2nd Adder 17).

Yoshida teaches that the branch offset is calculated by adding an offset to the address of the instruction following the branch instruction. This occurs by adding a "Word Length" that is part of the instruction decoded (Figure 2 and column 4, lines 1-20)

12. It would have been obvious to add the hardware of Yoshida to implement the branch target address computation because hardware is inherently necessary in order to carry out the x86 relative branch instructions and because the invention of Yoshida eliminates time required by conventional processors to do branch target calculations (Abstract).

13. While Goetz, in view of Yoshida, teaches a method for handling the x86 branch instruction, it is still necessary to have hardware to implement the PowerPC branch instruction. One of ordinary skill in the art would have recognized that since the purpose of the 1st adder of Yoshida is to add the

appropriate length of the branch instruction in order to complete the branch instruction that adds an offset to the address of the instruction following the branch instruction, in order to appropriately execute PowerPC branch instructions, it would be necessary to add a zero as the "word length" to properly calculate the branch target address. Adding a value other than zero as the "word length" while executing PowerPC branch instructions would result in an incorrect branch target address being calculated. Therefore, it would have been inherent to use a zero input as a word length in the system of Goetz, in view of Yoshida, while executing PowerPC-like branch instructions and to use the appropriate, non-zero value word length when executing the x86-like branch instructions.

14. However, Goetz in view of Yoshida fails to teach that the "Word Length" values, zero and non-zero values, are stored in a memory and selected via a multiplexer with said parameter as an input.

15. Since Goetz already teaches a parameter indicating which instruction set's offset to add to the program counter for sequential instruction fetching, one of ordinary skill in the art would have recognized to use the same parameter to indicate which offset to add for different non-sequential instruction fetching, i.e., the branch instructions of each instruction set, in order to avoid redundant hardware.

16. Furthermore, since the combination of Goetz and Yoshida presents a system in which two instruction sets with two respective branch target address generation schemes are implemented, and in which a Q-bit (Goetz) is already used to indicate which instruction set addressing mode is to be used for a

particular instruction, and no hardware implementation has been provided by Yoshida to describe how the "word length" value is generated, one of ordinary skill in the art would have recognized to use a multiplexor to select which one of the two "word length" value types is needed (zero or variable) to present using the Q-bit as the selecting parameter. To further clarify, the combination of Goetz and Yoshida presents a problem of needing to select between two different values for the "word length", one being a zero for PowerPC-like branch instructions, and the other being the normal "word length" used for the x86-like branch instructions. One of ordinary skill in the art would have recognized that a multiplexers function is to select between two options using a controlling parameter (as evidenced by Section 3-7 of Logic and Computer Design Fundamentals, Kime), and since Goetz already teaches the Q-bit being used to indicate to hardware throughout the system which instruction set is currently being executed (x86 or PowerPC), it would have been obvious to use the Q-bit as the selecting parameter input to the multiplexer. Using the multiplexer would provide the advantage of solving the inherent problem of providing the correct "word length" to the 1st adder in figure 2, either a zero or the "word length" that would otherwise be provided when not executing PowerPC-like branch instructions.

17. As per claim 4, Goetz, in view of Yoshida and Borar fail to teach the only limitation different from claim 3, which is "a subtracting unit" instead of an "adding unit."

18. However, Examiner takes Official Notice that numbers, including offsets, are very frequently represented in two's complement form, which allows simplified binary arithmetic operations.

19. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the offsets represented in two's complement form since Examiner takes Official Notice two's complement form allows simplified binary arithmetic operations.

20. It is inherent that a binary adder is also a subtraction unit if the binary inputs are in two's complement form, because there is no difference in hardware between adding two's complement numbers and subtracting two's complement numbers. A two's complement adder is inherently a subtraction unit as well.

Response to Arguments

21. Applicants arguments filed on 2/10/06 have been fully considered but they are not persuasive. The majority of arguments are moot in view of the new rejections above, however, pertinent arguments regarding specific references are responded to below.

22. Applicant argues the novelty/rejection of claims 3 and 4.

> "Contrary to Applicants' claimed invention, a **complicated cascade of adding units** is necessary in Yoshida, **in order to compute the correct value for determining the relative address on the basis of the program code**. Thus, Yoshida, like Goetz fails to teach or suggest, among other limitations of Applicants' claims, the controlled supplying of instruction word lengths or the value 'o', to a multiplexer, in dependence upon which assembler code is selected. "

23. These arguments are not found persuasive for the following reasons:

a. To clarify, applicant's attention is directed towards Applicant's own figures and claims. From claim 3,

i. "a multiplexer...a computation unit...[and] an adding unit connected between said program counter and said computation unit, said adding unit having...an output connected to said computation unit."

b. The specification does not clarify exactly what the computation unit is, however, as it is believed to be taking in the appropriate PC and then to compute a branch target address, the computation is assumed to be either an addition or a subtraction. Therefore, Applicant's invention would also be a "complicated cascade of adding units" and it is unclear the distinction that Applicant is attempting to make.

c. Furthermore, it is unclear what constitutes a "complicated" cascade of adding units, since Examiner submits that two adding units connected together does not inherently result in a "complicated" circuit.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571) 272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

KPR

EDDIE CHAN
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